

UNDER 35 USC 371

5397432

SERIAL
NUMBER
(Series
of 1987)

743353

PATENT DATE

AUG 12 1995

PATENT
NUMBER



NUMBER 43,393	FILING DATE 08/21/91	CLASS 156	SL CLASS 156 665	GROUP ART UNIT 1109	EXAMINER Goudreau
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ON: CHI KONNO, MIE, JAPAN; KEISUKE SHINAGAWA, KANAGAWA, JAPAN;
OSHIYUKI TSHIDA, KANAGAWA, JAPAN; TAKAHIRO ITO, KANAGAWA, JAPAN;
TAKESHI KONDO, KANAGAWA, JAPAN; FUKASHI HARADA, MIE, JAPAN; SHUZO
UJIYURA, TOKYO, JAPAN

36kt

CONTINUING DATA
VERIFIED

gag 9-92

*****PCT APPLICATIONS*****

VERIFIED PCT PCT/JF91/00861 06/26/91
JAPAN 2-171791 06/27/90

gag 9-94

claimed ditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	AS FILED	STATE OR COUNTRY JPX	SHEETS DRWGS. 7	TOTAL CLAIMS 22	INDEP. CLAIMS 4	FILING FEE RECEIVED \$560.00	ATTORNEY'S DOCKET NO. 911333
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Mr. NIKAIKO, MARCELSTEIN, MURRAY, DRAM

Metropolitan square
655 15th ST, N.W.
Suite 330 - G ST. Lobby
Wash. D.C. 20005-5701

FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS
IN SUCH METHOD

U.S. DEPT. of COMM-Pat. & TM Office - PTO-436L (Rev. 10-78)

ITS OF APPLICATION
AND SEPARATELY

NOTICE OF ALLOWANCE MAILED 9-16-94		PREPARED FOR ISSUE 9-28-94 George Goudreau Assistant Examiner Richard Docket Clerk		CLAIMS ALLOWED Total Claims 19 Print Claim 1	
ISSUE FEE Amount Due 170.00 Date Paid 12-9-94		R. BRUCE BRENNEMAN Supervisory Patent Examiner Art Unit 1109 Primary Examiner		DRAWING Sheets Drwg. 6 Figs. Drwg. 13 Print Fig. 9	
Label Area		ISSUE CLASSIFICATION Class 156 Subclass 665		ISSUE BATCH NUMBER E51	

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